

Course Material Submission Form

OAN Match Definition Form

Today's Date: 1-30-08

Use this table to specify institutional data	
College/University:	Shawnee State University
Name and title of individual submitting on behalf of the college/university	
Name:	Dave Todt, PH.D
Title:	Associate Provost
Address:	940 Second Street, Portsmouth Oh 45662
Email:	dtodt@shawnee.edu
Phone:	740.351.3175
Fax:	740.351.3501

Indicate the reason for this submission:

New Course Match
 Revised Materials - Faculty review panel requested clarification
 Revised Materials - Institution submitting additional information
 Revised Materials - Course content revised by institution, including situations of both content and credit hour change
 Revised Materials - Other

Describe specific revisions being made for "Revised Materials" submissions:
 Conversion from Quarters to Semesters.

Institutional Notes to Faculty Panel (the institution is encouraged to add any additional clarifications for this submission):

Please see Additional Documentation for the requested information.

Table 1 – Use this table to describe the course match for which materials are being submitted for the first time or revised.

Proposed effective year and term of match (Final effective date will depend on actual approval of match by faculty panel. Effective Year and Term is the first term in which students taking the course will receive matching credit.)

Semester institutions complete this row:
 2007 Academic Year Summer Autumn Spring

Quarter institutions complete this row:
 20 Academic Year Summer Autumn Winter Spring

Ohio Articulation	OET002
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Number (OAN) (Use a separate form for each OAN.):	
Number of courses in the match:	1 (up to 10)
Current status of match:	<input type="checkbox"/> First time submission
	<input type="checkbox"/> Approved <input type="checkbox"/> Submitted <input type="checkbox"/> Disapproved <input type="checkbox"/> Error <input checked="" type="checkbox"/> Resubmitted <input type="checkbox"/> Pending <input type="checkbox"/> Error with enrollment <input type="checkbox"/> Not submitted
Course or Courses being matched to or currently matched to the OAN listed above. (Course Numbers must be exactly what will appear on a student's transcript.):	Course Number
	1. ETEM2212
	2.
	3.
	4.
	5.
	6.
	7.
	8.
	9.
10.	

Table 2 - Use this table to submit course materials for the first time or to revise previously submitted course materials. You must submit each course in a separate form, repeating the match definition information in Table 1 above for each form submitted.					
Course Number. (Course Numbers must be exactly what will appear on a student's transcript.):		ETEM2212	Course Title:		Digital Logic
Hours (be sure that the hours for this course matches the hours in the OAN.)					
<input checked="" type="checkbox"/> Semester Hours			<input type="checkbox"/> Quarter Hours		
Total Credit Hours	4	Lecture Hours	3	Laboratory Hours (if applicable)	3
Course Placement in Major:			<input type="checkbox"/> Major Requirement <input type="checkbox"/> Major Elective <input type="checkbox"/> Other		
Pre-Requisite Course work (if applicable) (Be sure this is consistent with the OAN definition): ETEM 1216 Electronics					
Catalog/Course Description: ETEM2212 Digital Logic: Introduction to solid state, integrated electronic logic, practical applications of Boolean Algebra, logic gates, binary pulse circuits, number systems, and computer arithmetic. Integrated circuit applications which include combinational and sequential logic, printed circuits, counters, registrers, decoders, signal converters, and an introduction to microcomputers.					
Texts/Outside Readings/Ancillary Materials (Be sure that the text meets performance expectations):					

Digital Systems: Principles and Applications, Ronald J Tocci

Course Objectives and/or Plan of Work:

(Provide a clear indication of how the course objectives align with the matched OAN's learning outcomes. This will facilitate the faculty panel course review process.)

GOALS AND OBJECTIVES:

The goal of the course is to familiarize the student with basic electronic logic concepts and practices. The applications of solid state logic devices, discrete and integrated, will be emphasized. An introduction to microcomputers will also be studied.

The student will achieve the following learning objectives provided he/she follows and completes the prescribed course format:

1. Demonstrate capability of analyzing, designing and troubleshooting:
 - a) discrete and integrated switching and logic circuits.
 - b) discrete and integrated regenerative circuits.
2. Be capable of performing basic switching analysis by using Boolean Algebra.
3. Be capable of applying computer arithmetic.
4. Demonstrate the use of digital integrated circuits in semi-sophisticated applications.
5. Be capable of performing semi-sophisticated circuit design and troubleshooting in using integrated elements.
6. Through laboratory utilization gain a basic familiarization with the operation of microcomputers.
7. Have a working knowledge of printed circuit techniques.
8. Experience a positive change in professional confidence and thinking ability.
9. Experience a positive change in creativity.

INSTRUCTIONAL DELIVERY METHOD

The majority of the instruction will be of lecture type. Students will be permitted questions and discussion times during the lectures. The lectures will be structured but will be semi-formal. Overhead transparencies will accompany nearly all lectures. Several lectures will be accompanied by appropriate demonstrations. Some lecture time will be utilized for the purpose of in-class special assignments. Special assignments may be given for both in and out of class work.

During the lecture development for each chapter, suggested problem assignments will be given. The purposes of these assignments is to give the student the opportunity to enhance the learning process for the particular subject being presented in the lectures. At an appropriate time, problem assignment solutions will be provided to the student. Do not consider these problems as "homework". They will not be collected, graded and returned. However, the subject content of the problems will be used for the development of quizzes and exams.

Laboratory Component:

The nature of the laboratory component is more subjective than objective. Items

such as attendance, attitude, ability to work with others, confidence, cooperation, performance, safety, organization, and use of time comprise the material for course grade consideration.

Description of Assessment and/or Evaluation of Student Learning (The

assessment plan needs to be appropriate for the expected rigor of the course) :

GRADING SYSTEM

Exams	20%
Final Exam	30%
Pop Quizzes	15%
Lab Performance	25%
Attendance	10%
TOTAL	100%

GRADING SCALE:

A	95-100
A-	91-94
B+	87-90
B	83-86
B-	79-82
C+	75-78
C	71-74
C-	67-70
D+	63-66
D	59-62
D-	55-58
F	00-54

Master Syllabi and Working Syllabi (if both are used):

TOPICS TO BE COVERED:

1. Introduction to Digital Logic
2. Number systems
3. Logic Gates
4. Boolean Algebra
5. Combinational Logic Circuits
6. Flip-Flops
7. Digital Arithmetic
8. Operations and Circuits
9. Counters, Registers
10. IC Logic Families
11. MIS Logic
12. Interfacing

- 13. Memory Devices
- 14. Programmable Logic Devices
- 15. Microprocessor

Additional Documentation:

SHAWNEE STATE UNIVERSITY
COURSE SYLLABUS

ETEM 2212

Digital Logic

Instructor Carl Priode Phone 740-351-3368
Office ATC 324 E-mailcpriode@shawnee.edu
Office Hours Tba Dept. Industrial & Engineering Technologies

Credit Hours:

3 lecture 3 lab 4 credit hours

This course is a combination of two 4 credit hour quarter courses into one 4 credit hour semester course with compression of material.

Class Location and Meeting Times:

Lecture – ACT 201 Lab – ATC 304

Materials Needed:

Digital Systems: Principles and Applications, Ronald J. Tocci

Course Description:

ETEM 2212, Digital Logic (4) – Introduction to solid state, integrated electronic logic, practical applications of Boolean Algebra, logic gates, binary pulse circuits, number systems, and computer arithmetic. Integrated circuit applications which include combinational and sequential logic, printed circuits, counters, registers, decoders, signal converters, and an introduction to microcomputers. Preq. ETEM 1216. 3 lec. 3 lab. \$ E T.

Goals and Objectives:

The goal of the course is to familiarize the student with basic electronic logic concepts and practices. The applications of solid state logic devices, discrete and integrated, will be emphasized. An introduction to microcomputers will also be studied.

The student will achieve the following learning objectives provided he/she follows and completes the prescribed course format:

- Recognize number systems, operations and codes.
- Describe function of basic logic gates. e.g. AND, OR, EXOR, NOR, NAND
- Demonstrate capability of analyzing, designing and troubleshooting: a) discrete and integrated switching and logic circuits; b) discrete and integrated

regenerative circuits.

- Be capable of performing basic switching analysis by using Boolean Algebra.
- Use Boolean algebra to simplify and reduce boolean expressions to minimize digital circuitry.
- Implement combinational logic circuits using expressions derived from using DeMorgan's theorem and Karnaugh maps.
- Be capable of applying computer arithmetic
- Define the function of encoders and decoders and describe typical applications.
- Define the function of multiplexers and demultiplexers and describe typical applications such as serial and parallel data conversion for both input and output data.
- Define the function of adders, subtractors, and Arithmetic Logic Units (ALU).
- Describe the various types of flip-flops (R-S, J-K, D), latches, and related devices and illustrate typical applications.
- Introduction to counter and register circuits. Analysis of various mod configurations for counters.
- Define characteristics of the various logic families and IC circuit technologies.
- Describe semiconductor memory circuits and addressing schemes.
- Define characteristics of microprocessors and discuss differences with computers and microcontrollers.
- Discuss aspects of Programmable Logic Devices and other VHDL circuits and describe typical applications.
- Demonstrate the use of digital integrated circuits in semi-sophisticated applications
- Be capable of performing semi-sophisticated circuit design and troubleshooting in using integrated elements.
- Through laboratory utilization gain a basic familiarization with the operation of microcomputers
- Have a working knowledge of printed circuit techniques
- Experience a positive change in professional confidence and thinking ability
- Experience a positive change in creativity

Student Responsibilities

Two exams

ATTENDANCE POLICY: Attendance is decided entirely by the student, but regular attendance is advised. For the purpose of evaluation, attendance will be recorded.

All cell phones and lap top computers will be turned off and put away during lecture.

SAFETY: The safety of all class participants is of primary concern and takes precedence over all other considerations. All participants must act responsibly and operate equipment in a safe way, consistent with written and verbal instructions. Deliberate misuse of equipment, failure to follow safety procedures, or any horseplay will result in immediate disciplinary action. No drinking, eating, or use of tobacco products is allowed in classrooms or laboratories.

University Disability Statement

For students who have a specific physical, psychiatric, or learning disability and require accommodations, please let me know early in the quarter so that your learning needs may be appropriately met. By law, it is your responsibility to provide documentation of your disability to the Office of Disability Services, located in the Student Success Center, Massie Hall, (Ph) 351-3594, PRIOR to receiving services.

Evaluation:

GRADING SYSTEM: GRADING SCALE

Exams	20%	95-100	A	71-74	C
Final Exam	30%	91-94	A-	67-70	C-
Pop Quizzes	15%	87-90	B+	63-66	D+
Lab Performance	25%	83-86	B	59-62	D
Attendance	10%	79-82	B-	55-58	D-
	100%	75-78	C+	00-54	F

Instructional Delivery Method:

The majority of the instruction will be of lecture type. Students will be permitted question and discussion times during the lectures. The lectures will be structured but will be semiformal. Overhead transparencies will accompany nearly all lectures. Several lectures will be accompanied by appropriate demonstrations. Some lecture time will be utilized for the purpose of in-class special assignments. Special assignments may be given for both in and out of class work.

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LABORATORY COMPONENT: The nature of the laboratory component is more subjective than objective. Items such as attendance, attitude, ability to work with others, confidence, cooperation, performance, safety, organization, and use of time comprise the material for course grade consideration.

Licensure or Accreditation Statement

N/A

Topics to be Covered

- Introduction to Digital Logic
- Number Systems

- Logic Gates
- Boolean Algebra, DeMorgan's Theorem, Karnaugh maps.
- Combinational Logic Circuits
- Flip-Flops
- Digital Arithmetic
- Operations and Circuits
- Counters, Registers
- IC Logic Families

- MIS Logic
- Interfacing
- Memory Devices and addressing schemes
- Programmable Logic Devices
- Microprocessor

OBR Use

Approved-Effective Date	
Pending (i.e. Additional Information Requested)	
Disapproved	
Today's Date	

Course Material Submission Form

Instructions and notes

1. Submit completed forms to atpanels@regents.state.oh.us.
2. Use this form to define course matches and to submit new or revised course materials for faculty panel review. Please do not submit a form for multiple OANs or Courses.
3. For course renumbering and credit hour revision, remember to withdraw the old match.
4. For course renumbering and credit hour revision, you may want to include information about how the new numbers relate to the old in the Institutional Notes to the Faculty Panel.
5. Click check boxes to check the item. Text fields will expand as you enter information. Press tab to move forward through form. Press Shift-tab to move backward. Note that these tables are implemented as MS Word tables. Keep that in mind as you are copying and pasting between your syllabi and this form. It is possible to paste tables as nested tables. Use the Edit Menu "Paste as Nested Tables" selection.
6. Once you are done entering your information, save the data file. Under the File menu, choose "Save as" and then enter the name (no spaces!) of the file using the following naming conventions:
 - a. For course material submissions: **Institution-OAN-Course Number-Sequence-Version. Institution** is the 4 character HEI institution designation. **OAN** is the Ohio Articulation Number whose match is being defined or revised. **Course Number** is the **transcript** course number. **Sequence** is an indication of which course of a multi-course match is addressed in this form. The sequence is of the form (n of m) for an m-course match. For example, 1 of 1 for a single course match or 1 of 2 and 2 of 2 for a 2 course match. **Version** is a number indicating the revision number of this submission. Start with "Ver1" for the first time submission and include the "Ver".

Example:

If you are submitting course materials for Rhodes Community College MATH110 for OMT005 the name of the file would be LMTC-OMT005-MATH110-(1 of 1)-Ver1.

If you are submitting course materials for Rhodes Community College MATH111 and MATH112 for OMT006 the name of the files would be LMTC-OMT006-MATH111-(1 of 2)-Ver1 and LMTC-OMT006-MATH112-(2 of 2)-Ver1.

7. Course materials must be submitted according to timelines below:

Considering the submissions of **new** courses for TAG matches, our goal is to work toward a timeline as follows:

Submit Course Material:	Start of Term 1
Faculty Panels Review Submitted Courses:	During Term 1
Approved course is effective:	Start of Term 2
Approved course is matched for transcript processing:	Term 3

A new match will have to be approved according to the timeframes below:

Course Approval Sample Timelines

Quarter Institutions

	Summer	Autumn	Winter	Spring
Course Material Submitted for Review	By 6/1	By 8/15	By 1/1	By 3/1
Faculty Panel Reviews Completed	By 8/1	By 12/31	By 2/28	By 5/31

Semester Institutions

	Summer	Autumn	Spring
Course Material Submitted for Review	By 6/1	By 8/15	By 1/1
Faculty Panel Reviews Completed	By 8/1	By 12/31	By 5/31

- Remember that all institutions are required to have at least one course match for each OAN in all TAGs for which they have corresponding programs.
- This form should be used for all submissions or resubmissions starting immediately.
- If you encounter problems or have questions, please contact any of the individuals listed below:

Jim Ginzer (614) 752-9486 jginzer@regents.state.oh.us
 Sam Stoddard (614) 752-9532 sstoddard@regents.state.oh.us
 Brett Berliner (614) 466-2004 bberliner@regents.state.oh.us